AN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,049	07/18/2001	Suresh Katukam	CISCP694	8487

54406 7590 11/15/2005

AKA CHAN LLP / CISCO
900 LAFAYETTE STREET
SUITE 710
SANTA CLARA, CA 95050

EXAMINER	
CHEA, PHILIP J	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,049	KATUKAM ET AL.	
	Examiner	Art Unit	
	Philip J. Chea	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-11,19-27 and 37-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,19-27,37-42 and 44* is/are rejected.

7)☒ Claim(s) *43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to a Request for Continued Examination filed on September 27, 2005. Claims 1-6,8-11,19-27,37-44, are currently pending, of which claims 39-44 are new. Any rejection not set forth below has been overcome buy the current Amendment.

Claim Objections

1. Claim 44 is objected to because of the following informalities:

2. Note line 4, "form" is apparently "from";

   Note line 7, "specify at circuit" is apparently "specify circuit";

   Note line 10, "element" is apparently "elements"

3. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   > The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-6,8-11,19-27,37-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "the group" in line 8. There is insufficient antecedent basis for this limitation in the claim. The Examiner will not recognize

7. Claim 19 recites the limitation "the group" in line 8. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 24 recites the limitation "the group" in line 8. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 39 recites the limitation "the group" in line 8. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 44 recites the limitation "the group" in line 4. There is insufficient antecedent basis for this limitation in the claim.

11. Any claims not mentioned specifically are rejected by virtue of being dependent on a rejected claim.

12. Appropriate correction is required.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-3,5,8-11, 19, 21-23, 24, 26, 27, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allen (U.S. 2001/0032271), and further in view of Dravida et al. (US 5,253,248), herein referred to as Dravida.

As per claims 1, Allen discloses a system for computing paths between a first node and a second node within a network (see column 9, lines 21-23, where optical network is implied), as claimed, comprising:

- a memory (see paragraph [0030], where a route digest as a Bloom filter implies a memory);
- a route generator being arranged to generate a primary circuit path between the first node and the second node, the primary path including a first element selected from the plurality of elements (see paragraphs [0025-0026], where primary path is considered working path, and first node is considered originating node, and second node is considered destination node); wherein the route generator is arranged to accept an input,

the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for the alternate circuit path (see paragraphs [0037-0038]); and

- a list mechanism, the list mechanism being stored in the memory, the list being arranged to identify the first element, wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first element identified by the list mechanism and a failure of the first element does not affect generating the alternate circuit path (see paragraphs [0037-0038]).

Although the system disclosed by Allen shows substantial features of the claimed invention (discussed above), it fails to disclose an input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Allen, as evidenced by Dravida.

In an analogous art, Dravida discloses a system to avoid spreading congestion by implementing alternate paths, further showing an input being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path (see Fig. 22 for primary path and Fig. 24 for alternate path, wherein circuit characteristics include shortest distance considerations).

Given the teaching of Dravida, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Allen by employing a shortest distance path routing scheme, such as disclosed by Dravida, in order to reduce the amount of time it takes for traffic to go from a sender and recipient node).

As per claims 2, Allen in view of Dravida discloses a system, as claimed, wherein the first element is a link (see Allen paragraphs [0025-0026], and Fig. 1, where links are used to connect between the originating node and the destination node).

As per claims 3, Allen in view of Dravida discloses a system, as claimed, wherein the first element is a node (see Allen paragraphs [0025-0026]).

As per claim 5, Allen in view of Dravida discloses a system, as claimed, wherein the route generator is arranged to generate the primary circuit path that includes the first element and a set of elements (see Allen paragraphs [0025-0026]), and the list mechanism is arranged to identify the first element and the set of elements as being inaccessible for use in generating the alternate circuit path (see Allen paragraphs [0037-0038]).

As per claim 8, Allen in view of Dravida discloses a system, as claimed, wherein when the input specifies the nodal diverse constraint, the first element is a node (see Allen paragraphs [0037-0038]).

As per claim 9, Allen in view of Dravida discloses a system, as claimed, wherein when the input specifies the link diverse constraint, the first element is a link (see Allen paragraphs [0037-0038], where nodes are separated by links).

As per claim 10, Allen in view of Dravida discloses a system, as claimed, wherein the device is associated with the first node (see Allen paragraph [0021]).

As per claim 11, Allen in view of Dravida discloses a system, as claimed, wherein the route generator is further arranged to implement the primary circuit and the alternate circuit path (see Allen paragraphs [0025-0026] and paragraphs [0037-0038], where it is implied the circuits are implemented once the routing decisions are made).

As per claims 19 and 24, Allen in view of Dravida discloses an element for use in an optical network, the optical network including a plurality of links, the element comprising:

a memory (see Allen paragraph [0030], where a route digest as a Bloom filter implies a memory);

a route generator, the route generator being arranged to compute a first circuit path between the element and the destination node, the first circuit path including a first link included in the plurality of links (see Allen paragraphs [0025-0026]), wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for a second circuit path between the element and the destination node (see Allen paragraphs [0037-0038]), the input further being arranged to specify circuit characteristics for the first

circuit path and for the second circuit path (see Dravida Fig. 22 for primary path and Fig. 24 for alternate path, wherein circuit characteristics include shortest distance considerations); and

a list, the list being stored in the memory, the list including a plurality of identifiers, the plurality of identifiers being arranged to identify selected links included in the plurality of links, the plurality of identifiers including a first identifier that identifies the first link, wherein the route generator is further arranged to compute the second circuit path using the list and the input, wherein the second circuit path includes a second link included in the plurality of links and does not include the selected links identified by the plurality of identifiers included in the list, wherein a failure of any of the selected links identified by the plurality of identifiers included in the list does not affect computing of the second circuit path (see Allen paragraphs [0037-0038]).

As per claim 21, Allen in view of Dravida further discloses a system, as claimed, wherein the element described in claim 19 is a source node (see Allen paragraph [0022]).

As per claim 22, Allen in view of Dravida further discloses a system, as claimed, wherein route generator identifies a first link to place in the list (see Allen paragraph [0036]).

As per claim 23, Allen in view of Dravida further discloses identifiers that are arranged to identify the selected links included in the plurality of links and to place the plurality of identifiers that are arranged to identify the selected links included in the plurality of links in the list [see Allen paragraph [0039]).

As per claim 26, Allen in view of Dravida further discloses an element applied to claim 23 above as a source node (see Allen column 7, lines 46-60, where transporting data implies the node being a source to another object on the network).

As per claim 27, Allen in view of Dravida further discloses an element applied to claim 23 above to place the first identifier that identifies the first node in the list (see Allen columns 7 and 8, lines 65-67 and 1-12, where failure types can be links or nodes and the implied list is used to remember the location and type of failure).

As per claim 37, Allen in view of Dravida further discloses that the route generator is arranged to generate the primary circuit path and the alternate circuit path as nodal diverse paths in which the primary circuit path and the alternate circuit path have substantially no common nodes between the first node and

the second node, and wherein when the primary circuit path and the alternate circuit path are the nodal diverse paths, the first element is a node (see Allen paragraphs [0037-0039]).

As per claim 38, Allen in view of Dravida further discloses that the route generator is arranged to generate the primary circuit path and the alternate circuit path as link diverse circuit paths in which the primary circuit path and the alternate circuit path share substantially no links between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the link diverse circuit paths, and the first element is a link (see Allen paragraphs [0037-0039]).

15. Claims 4,6,20,25,39-42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allen in view of Dravida as applied to claims 1, 5, 12,19,24 above, and further in view of Applicant's admitted Prior Art.

As per claims 4,6,20 and 25, Allen in view of Dravida discloses means for identifying the link as being inaccessible to the alternate circuit path, wherein the means for including the identifier which identifies the first element as being inaccessible for use as a part of the alternate circuit path is arranged to include an identifier which identifies the link as being inaccessible to the alternate circuit path in the list.

Although the system disclosed by Allen in view of Dravida shows substantial features of the claimed invention (discussed above), it fails to disclose the link being a protected link.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Allen in view of Dravida, as evidenced by the Applicant.

In an analogous art, the Applicant discloses that it is old and well known in the art to have a network that contains protected links (see Specification page 2, lines 17-27). Further it would have been obvious to modify Allen in view of Dravida by enabling the alternate circuit path to avoid the protected link and identify it as being inaccessible in order to avoid the high costs incurred of traversing the protected link.

As per claim 39, Allen in view of Dravida in view of Applicants admitted Prior Art discloses a memory (see Allen paragraph [0030], where a route digest as a Bloom filter implies a memory);

a route generator being arranged to generate a primary circuit path between the first node and the second node, the primary path including a first element selected from the plurality of elements (see Allen paragraphs [0025-0026], where primary path is considered working path, and first node is considered originating node, and second node is considered destination node), wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for the alternate circuit path (see Allen paragraphs [0037-0038]), the input further being arranged to specify a load characteristic that is to be accounted for when the alternate circuit path is generated (see Dravida column 10, lines 41-52); and

a list mechanism, the list mechanism being stored in the memory, the list being arranged to identify the first plurality of elements and at least one protected element (see discussion above regarding Applicants admitted Prior Art), wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first plurality of elements and at least one protected element identified by the list mechanism (see Allen paragraphs [0037-0038], and discussion above regarding Applicants Prior Art).

As per claim 40, Allen in view of Dravida in view of Applicants admitted Prior Art further discloses the first plurality of elements are link diverse constraint (see Dravida column 10, lines 41-52).

As per claim 41, Allen in view of Dravida in view of Applicants admitted Prior Art further discloses that the first plurality of elements are nodes if the input specifies a nodal diverse constraint (see Dravida column 10, lines 16-21).

As per claim 42, Allen in view of Dravida in view of Applicants admitted Prior Art further discloses that the list mechanism is a tabular list (see Dravida Fig. 21, where a routing table is generated).

As per claim 44, Allen in view of Dravida further disclose a device for computing circuit paths between a first node and a second node within a network, the network including a first plurality of elements and at least one protected element (see discussion for protected elements above), the device comprising:

a memory (see Allen paragraph [0030], where a route digest as a Bloom filter implies a memory);

a route generator, the route generator being arranged to generate a primary circuit path between the first node and the second node, the primary circuit path including the first plurality of elements (see Allen paragraphs [0025-0026], where primary path is considered working path, and first node is considered originating node, and second node is considered destination node), wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for the alternate circuit path (see Allen paragraphs [0037-0038]), the input further being arranged to specify a load characteristic that is to be accounted for when the alternate circuit path is generated (see Dravida column 10, lines 41-52); and

a list mechanism, the list mechanism being stored in the memory, the list mechanism being arranged to identify the first plurality of elements and the at least one protected element (see discussion above regarding Applicants admitted Prior Art), wherein the route generator is further arranged to generate and alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the plurality of elements and the at least one protected element identified by the list mechanism (see column 9, lines 17-67 and column 10, lines 1-40).

Allowable Subject Matter

16. Claim 43 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

17. Applicant's arguments in regard to a list mechanism stored in memory for claims 1,19,24 have been fully considered but they are not persuasive. However, new art has been applied to the Amendments not discussed below.

(A) Applicant contends that Allen does not teach a list mechanism stored in memory.

(B) Applicant contends that Allen does not teach an input that specifies any constraint.

In considering (A), the Examiner respectfully disagrees. Allen discloses that the Bloom filter is used to store the route digest as a bit map. This bit map is inherently stored in memory. The examiner believes that the bit map is considered a list because each series of bits represents a route, and more than one route can be represented creating a list for the series bits. The claim does not require a particular type of list. Therefore, the Examiner takes the broadest interpretation of a list.

In considering (B), the Examiner respectfully disagrees. The Examiner does not believe that the claim language is clear enough to indicate that the input specifying a nodal diverse constraint and a link diverse constraint specifies constraining a second path to not include nodes from a first path and constraining a second path to not include links from a first path, respectfully. It is unclear if all elements must be different, or if only some elements must be different from the primary path. The Examiner is also concerned that the claim could be interpreted as having an input that specifies a nodal diverse constraint OR a link diverse constraint rather than an input that is able to give an option to pick among a nodal diverse constraint and a link diverse constraint. If the claim is interpreted as an input that specifies a nodal diverse constraint OR a link diverse constraint, then a system that specifies only a nodal diverse constraint could still read on the claim. Of course, the same would be true for a system that specifies only a link diverse constraint.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip J. Chea whose telephone number is 571-272-3951. The examiner can normally be reached on M-F 7:00-4:30 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Philip J Chea
Examiner
Art Unit 2153

PJC 11/7/05

GLENTON B. BURGESS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100